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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/859,575
Filing Date	05/15/2001
First Named Inventor	HAMILTON, JR., William J.
Art Unit	2878
Examiner Name	YAM, S.
Attorney Docket Number	00W071

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [x] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

Ack. receipt postcard

Remarks

Appeal Brief submitted in triplicate

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	William C. Schubert (Reg. No. 30,102)
Signature	William C Schubert
Date	MARCH 15, 2004

CERTIFICATE OF TRANSMISSION/MAILING

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Typed or printed name	William C. Schubert		
Signature	William C Schubert	Date	MARCH 16, 2004

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/859,575
Filing Date	05/15/2001
First Named Inventor	HAMITLTON, JR. William J.
Examiner Name	YAM, S.
Art Unit	2878
Attorney Docket No.	00W071

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0616

Deposit Account Name: RAYTHEON COMPANY

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

Name (Print/Type)	William C. Schubert	Registration No. (Attorney/Agent)	30,102	Telephone	805-562-2108
Signature	William C Schubert			Date	2004-03-15

(Complete *(if applicable)*)

In duplicate

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PD-00W071

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	)	
WILLIAM J. HAMILTON, JR. et al.	)	GAU: 2878
Ser. No. 09/859,575	)	Examiner:
Filed: May 15, 2001	)	S. Yam
For: HYBRID MICROELECTRONIC ARRAY	)	
STRUCTURE HAVING ELECTRICALLY ISOLATED	)	
SUPPORTED ISLANDS, AND ITS FABRICATION	)	

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant files its Appeal Brief in triplicate, together with a Fee Transmittal authorizing the charging of the required fee. A Notice of Appeal and fee were previously filed.

Real Party in Interest

The Real Party in Interest is the assignee, Raytheon Co.

Related Appeals and Interferences

Applicant is not aware of any related appeals and/or interferences.

Status of Claims

Claims 1-23 were filed. During prosecution, claims 15, 20, and 21 were amended. A clean copy of the claims, as amended, is found in the Appendix hereto.

Status of Amendments

A Response to the final rejection was filed, but it contained no amendments to the claims.

Summary of Invention

This invention deals with a hybrid microelectronic array (title). In an example, one widely used detector array is the focal plane array (FPA), in which an array of detector elements is positioned at the focal plane of the optical system. The infrared or visible-light energy focused onto the detector elements is converted to electrical signals. The electrical signals responsive to the image are viewed on a display or processed by a computer, as for example with pattern recognition techniques. The most sensitive FPA detector arrays are hybrid structures that use an optimized detector array and an optimized readout integrated circuit. The detector elements of the detector array are arranged to define pixels of an image and convert the incident infrared or visible-light energy to output electrical signals. (Specification, para. [0003]-[0004]) However, the present approach has limitations, particularly on the possible geometries of the FPA.

Claim 1 is illustrative of the present approach, Figure 1 illustrates the present structure, and para. [0021]-[0030] describe the present structure. A hybrid microelectronic array structure (20) includes an array of microelectronic integrated circuits (24). Each of the microelectronic integrated circuits has a first supported-structure interconnect location (30) and a second supported-structure interconnect location (32).

A supported array includes an array of supported islands (39). Each supported

island (39) has at least one supported element (38) therein. Each of the supported elements (38) has a first region (40) and a second region (42). The first region (40) of each of the supported islands is physically discontinuous from the first region (40) of each of the other supported islands. The second region (42) of each of the supported islands is physically discontinuous from the second region (42) of each of the other supported islands.

A bump interconnect structure (43) extends between each of the microelectronic integrated circuits (24) and its respective supported element (38). Each bump interconnect structure (43) has a first bump interconnect (44) extending from the first supported-structure interconnect location (30) of each of the microelectronic integrated circuits (24) to the first region (40) of its respective supported element (38). A second bump interconnect (46) extends from the second supported-structure interconnect location (32) of each of the microelectronic integrated circuits (24) to the second region (42) of its respective supported element. (That each of the different bump interconnects goes to a different region is a crucial point in the discussion of the applied prior art in the Argument below.)

This architecture allows the hybrid microelectronic array structure 20 to be planar or curved, an important advantage in many applications.

Issues

1. Are claims 1-3, 6, and 7 properly rejected under 35 USC 103 over Ozaki JP 06-037291?

2. Are claims 4 and 8-23 properly rejected under 35 USC 103 over Ozaki in view of Watton US Patent 6,388,256?

3. Is claim 5 properly rejected under 35 USC 103 over Ozaki in view of Shieh US Patent 5,621,225?

Grouping of Claims

The claims do not stand or fall together, except as stated next.

Under Issue 1, claim 2 stands or falls with claim 1.

Under Issue 2, claim 9 and claim 15 each stands or falls with claim 8.

Under Issue 2, claim 17 stands or falls with claim 16.

Arguments for separate patentability of the claims that do not stand or fall together is presented under Argument.

Argument

All references to the "final Office Action" are to the Office Action of July 18, 2003, in which the rejections of Issues 1-3 were made final.

Issue 1. Are claims 1-3, 6, and 7 properly rejected under 35 USC 103 over Ozaki JP 06-037291?

The following principle of law applies to all sec. 103 rejections. MPEP 2143.03 provides "To establish prima facie obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." [emphasis added] That is, to have any expectation of rejecting the claims over a single reference or a combination of references, each limitation must be taught somewhere in the applied prior art. If limitations are not found in any of the applied prior art, the rejection cannot stand. In this case, the single applied prior art reference clearly does not arguably teach some limitations of the claims.

Claim 1 recites in part:

"a first bump interconnect extending from the first supported-structure interconnect location of each of the microelectronic integrated circuits to the first region of its respective supported element, and

a second bump interconnect extending from the second supported-structure interconnect location of each of the microelectronic integrated circuits to the second region of its respective supported element."

Referring to the paragraph bridging pages 2-3 of the final Office Action, the portion of Ozaki that is read upon the claimed "first region" is the n-type layer 3, and the portion of Ozaki that is read upon the claimed "second region" is the p-type layer 2. Applicant certainly agrees that there is a "second bump" 8 interconnect extending to the p-type layer 2, as shown in Figure 2(c) of Ozaki.

But there is no "...first bump interconnect extending...to the first region..." as recited in claim 1. The n-type layer 3 is not even shown in Figure 2(c) of Ozaki, so none of the bumps 8 or 8A or 8B are taught to extend to the n-type layer 3. The argument presented at page 10, lines 13-18 of the final Office Action is a construct that is unsupported in the facts. There is no disclosure or illustration suggesting that any of the bumps 8, 8A, or 8B extend to, contact, reach or otherwise have any relation to the n-type layer 3. The response asserts that the bump 8 "simply reaches the area of the first region", but a look at Figure 2(c) tells you it doesn't--nothing suggests that any of the bumps 8 reach the n-type layer 3, and in fact all of the bumps 8 terminate at the p-type layer 2. In fact, all that is needed is to count that there are 6 bumps 8 on the bottom in each group of Figure 2(c), and a corresponding 6 bumps 5 on the top in each group. Figure 2(c) clearly indicates that the 6 bumps 5 on the top are in communication with the p-type layer 2, leaving no top bumps 5 for communication with the n-type layer 3.

The explanation of the rejection seeks to focus on Figures 2a-c, and to capitalize on the possible ambiguity permitted by the fact that Figures 2a and 2b show the n-type layer 3, while Figure 2c does not. Of course, because Figure 2c does not show the n-

type layer 3, it cannot be presumed to have any particular relation to the bumps 5, and there can be no presumption that any of the bumps 5 connect to the n-type layer 3.

Further light is shed on the question of whether any of the bumps 5 extend to the n-type layer 3 by referring to the embodiment of Figure 4b, which does show both the n-type layer 3 and the p-type layer 2. As may be clearly seen in Figure 4b, the bumps 5 extend only to the p-type layer 2. None of the bumps 5 extend to the n-type layer 3.

"Extend" means "to reach, as to a particular point". The claim language recites the particular points: "a first bump interconnect extending from the first supported-structure interconnect location...to the first region of its respective supported element". "Reach" means "to succeed in touching", or "to stretch or extend so as to touch or meet" (All definitions set forth herein are evidentiary submissions from Webster's Unabridged Dictionary of the English Language, Portland House, 1989, and the relevant pages were submitted during prosecution). No bump 5 or bump 8 touches the n-type layer 3 in Ozaki. They touch the p-type layer 2, but never the n-type layer 3. The bump 5 and the bump 8 never extend to the n-type layer 3 under any formal or common-sense definition or concept.

This rejection relies on multiple assertions of "well known" prior art. "Well known" is not a class of statutory prior art recognized in 35 USC 102 or 35 USC 103. Applicant traverses this substitution of asserted "well known" prior art for a statutory prior art reference as applied in the context of the claim. When this assertion of "well known" prior art first was made, Applicant made a timely traverse and requested that, if the rejection was maintained, the Examiner apply a statutory prior art reference. MPEP 2144.03. Absent such an application of statutory prior art, Applicant requested that the rejection be withdrawn. The Examiner made no response to this traverse, which was made on two different occasions.

The final Office Action mentions but does not apply Bryan US Patent 6,458,547. Because this reference is not applied in forming the rejection, it cannot be relied upon in support of the rejection. If it were acceptable to rely on a reference that is not applied in forming the rejection, then it would never be necessary to cite the pertinent prior art so that the propriety of applying that art could be examined according to the applicable

legal principles.

In any event, Bryan '547 is a strange reference to apply to support what is asserted to be a "well known" modification to Ozaki's approach. Ozaki teaches a bump interconnect structure in an infrared detector. Bryan '547 has nothing to do with bump interconnect structures or infrared detectors, and has no teaching about either of these subjects. Bryan '547 teaches visible-light photodetectors that are preferably photodiodes (col. 40, lines 35-36), with no mention of any other type of detector structure. So Bryan '547 certainly does not support any assertion of what is "well known" in respect to bump interconnect structures in infrared detectors, as taught by Ozaki.

To the extent that there is an attempt to combine the teachings of Ozaki and Bryan, the present rejection seeks to perform a hindsight reconstruction based upon unrelated references, which is technically unsupported as discussed above and is legally improper. The case authority and the MPEP provide guidance on this point. The present rejection is a sec. 103 combination rejection. It is well established that a proper sec. 103 combination rejection requires more than just finding in the references the elements recited in the claim (but which was not done here). To reach a proper teaching of an article or process through a combination of references, there must be stated an objective motivation to combine the teachings of the references, not a hindsight rationalization in light of the disclosure of the specification being examined. MPEP 2143 and 2143.01. See also, for example, In re Fine, 5 USPQ2d 1596, 1598 (at headnote 1) (Fed.Cir. 1988), In re Laskowski, 10 USPQ2d 1397, 1398 (Fed.Cir. 1989), W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 311-313 (Fed. Cir., 1983), and Ex parte Levengood, 28 USPQ2d 1300 (Board of Appeals and Interferences, 1993); Ex parte Chicago Rawhide Manufacturing Co., 223 USPQ 351 (Board of Appeals 1984). As stated in In re Fine at 5 USPQ2d 1598:

> "The PTO has the burden under section 103 to establish a prima facie case of obviousness. [citation omitted] It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge

generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references."

And, at 5 USPQ2d 1600:

"One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."

Following this authority, the MPEP states that the examiner must provide such an objective basis for combining the teachings of the applied prior art. In constructing such rejections, MPEP 2143.01 provides specific instructions as to what must be shown in order to extract specific teachings from the individual references:

"Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention when there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992)."

* * * * *

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)."

* * * * *

"A statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were

> individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references. Ex parte Levengood, 28 USPQ2d 1300 (Bd.Pat.App.& Inter. 1993)."

Here, there is set forth no objective basis for combining the teachings of the references in the manner used by this rejection, and selecting the helpful portions from each reference while ignoring the unhelpful portions. An objective basis is one set forth in the art or which can be established by a declaration, not one that can be developed in light of the present disclosure. If the rejection is maintained, Applicant asks that the Examiner set forth the objective basis found in the references themselves for combining the teachings of the references.

The final Office Action argues, in the paragraph bridging pages 11-12, that it is not necessary to follow these MPEP and case law requirements, citing In re McLaughlin. The final Office Action asserts that "any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See In re McLaughlin, 443 F2d 1392, 170 USPQ 209 (CCPA 1971)." Applicant traverses this position. It is well established that hindsight reconstruction is not an acceptable basis for rejecting a patent claim.

Later cases from the Federal Circuit such as In re Fine 5 USPQ2d 1596, 1600 (Fed.Cir. 1988) have made it clear that hindsight reconstruction is not proper:

> "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."

Further on this point, the Federal Circuit in W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303 (Fed. Cir., 1983) has emphasized that

> "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." 220 USPQ 303, 312-313

In In re Mercer, 185 USPQ 774, 778 (CCPA 1975), the CCPA stated:

> "The Board's approach amounts in substance, to nothing more than a hindsight 'reconstruction' of the claimed invention by relying on isolated teachings of the prior art without considering the over-all context within which those teachings are presented. Without the benefit of appellant's disclosure, a person having ordinary skill in the art would not know what portions of the disclosure of the reference to consider and what portions to disregard as irrelevant, or misleading. See In re Wesslau, 53 CCPA 746, 353 F.2d 238, 147 USPQ 391 (1965)."

When first enunciated over 30 years ago, the position of In re McLaughlin might have been subject to differing interpretations. Those seeking support for rejecting patent applications could argue that the quoted language means that no motivation to combine teachings need be found in the prior art, and those seeking to gain allowance would argue to the contrary.

After this case was propounded, its legal principles were later explained and clarified by the Court of Appeals for the Federal Circuit, the successor to the CCPA. As stated in In re Fine, 5 USPQ2d 1596, 1599 (Fed.Cir. 1988):

> Obviousness is tested by 'what the combined teachings of the references would have suggested to those of ordinary skill in the art.' In re Keller, 208 USPQ 871, 881 (CCPA 1981). But it 'cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or

suggestion supporting the combination. ACS Hosp. Sys. [cite omitted]. And 'teachings of references can be combined only if there is some suggestion or incentive to do so.' Id. Here, the prior art contains none." [emphasis in original]

The language quoted by the Federal Circuit, 'what the combined teachings of the references would have suggested to those of ordinary skill in the art,' is substantially that relied on in forming the rejection from In re McLaughlin, except taken from a 1981 decision that sets forth the same principles, In re Keller.

The Federal Circuit then goes on to explain that "teachings of references can be combined only if there is some suggestion or incentive to do so. Here, the prior art contains none." [First emphasis in original, second emphasis added.] The Federal Circuit has thus held that the prior art itself must contain some suggestion or incentive to combine the teachings of the references, by way of clarifying the interpretation of cases like In re McLaughlin.

Applicant incorporates the discussion of the requirement for an object basis into each of the grounds of rejection that attempt to rely on more than one reference.

Turning to the other rejected claims, claim 2 stands or falls with claim 1.

Claim 3 recites in part:

"each microelectronic integrated circuit comprises
an electrical interface circuit, and
wherein each supported element comprises
an input/output element supported on the electrical interface circuit."

The final Office Action readily admits that "Ozaki et al. do not teach the circuit comprising an electrical interface circuit and an input/output element supported on the electrical interface circuit." (final Office Action, page 3, lines 4-5 from bottom of page) It is then asserted that it is "well known" to provide such recited features, but no supporting reference is set forth. The attempt to rely on Bryan '547 does not suggest

that Bryan '547 has any such features, and certainly Bryan '547 would not suggest such features in the context of the bump interconnect infrared detector structure of Ozaki.

Claim 6 recites in part: "the hybrid microelectronic array structure is planar". Ozaki has no such teaching. The recited "hybrid microelectronic array structure" includes the microelectronic integrated circuit array, the supported array, and the bump interconnect structure. Nowhere does Ozaki teach or illustrate that the structure formed of these three elements is planar. In each case taught by Ozaki, the element that corresponds to the supported array has a quasi curvature. The element that corresponds to the supported array is planar. The explanation of the rejection points to Figure 1 of Ozaki, but that structure is clearly not planar, because the supported array is curved.

Claim 7 recites in part: "the hybrid microelectronic array structure is curved". Ozaki has no such teaching. The recited "hybrid microelectronic array structure" includes the microelectronic integrated circuit array, the supported array, and the bump interconnect structure. Nowhere does Ozaki teach or illustrate that the structure formed of these three elements is curved. In each case taught by Ozaki, the element that corresponds to the supported array has a quasi curvature. The element that corresponds to the supported array is planar. The explanation of the rejection points to Figure 1 of Ozaki, but that structure is clearly not curved, because the microelectronic integrated circuit array is planar.

Issue 2. Are claims 4 and 8-23 properly rejected under 35 USC 103 over Ozaki in view of Watton '256?

Ozaki has been discussed above, and that discussion and the associated requests are incorporated here. These discussed points are relevant here because claim 4 depends from claim 1, and independent claims 8, 16, and 18 have similar relevant limitations and the same arguments are made in the explanations of the rejection.

Watton teaches a structure that is so different from that of Ozaki that Applicant cannot see how to interrelate their teachings. There is no "physically discontinuous" structure in Watton. The elements indicated in the explanation of the rejection to be an

"array of detector islands (5,8)" are in fact an interconnect layer 5 and electrically conducting channels or interconnect channels 8 (Watton, col. 5, lines 20-23). The electrically conducting channels 8 are holes or pores filled with an electrically conducting material (col. 5, lines 28-34). These filled holes or pores, commonly termed "vias" in the art, do not create isolated islands--they are simply holes through the otherwise continuous interconnect layer 5, much in the manner of a series of holes drilled through a flat sheet of plywood and which are then filled. They only appear to create isolated islands because the sectional view of the drawings is taken in the plane of the electrically conducting channels 8. The plan views of Figures 4-5 give a better idea of the continuous nature of the interconnect layer 5.

Thus, Applicant incorporates from the response to the first rejection the discussion of the failure of Ozaki to teach certain limitations of the claims. Watton adds nothing that would remedy these shortcomings of the teachings of the primary reference.

Additionally, Watton '256 cannot be applied as a reference. It is a well-established principle of law that a prima facie case of obviousness may not properly be based on a reference which teaches away from the present invention as recited in the claims.

> "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. In re Sponnoble, 160 USPQ 237 244 (CCPA 1969)...As "a useful general rule,"..."a reference that 'teaches away' can not create a prima facie case of obviousness." In re Gurley, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994)"

There is no doubt that Watton teaches away from the limitation of claim 1 "the first region of each of the supported islands is physically discontinuous from the first region of each of the other supported islands". The interconnect layer 5 of Watton '256 is a

continuous layer with the channels 8 therethrough. If a person of ordinary skill in the art is given both of these references and asked to determine, without knowledge of the present invention, whether the references teach a continuous or discontinuous layered structure, there is no way to make that determination. Watton '256 teaches directly contrary to what Ozaki teaches in this regard.

The present rejection seeks to perform a hindsight reconstruction based upon unrelated references, which is technically unsupported for the reasons stated above and is legally improper for the reasons stated in relation to this point under Issue 1, which are incorporated here. Here, there is set forth no objective basis for combining the teachings of the references in the manner used by this rejection, and selecting the helpful portions from each reference while ignoring the unhelpful portions. An objective basis is one set forth in the art or which can be established by a declaration, not one that can be developed in light of the present disclosure.

Once again, this rejection is based on an assertion of "well known in the art". The prior discussion of the law and the MPEP requirements relating to such an assertion is incorporated. Absent an application of statutory prior art, Applicant requested that the rejection be withdrawn. There was no application of prior art.

Claim 4 includes the recitations of claims 1 and 3, and the prior discussion of the rejection of these claims is incorporated here. Claim 4 further recites in part: "the electrical interface circuit is a readout integrated circuit, and the input/output element is a detector." The supported detectors in Watton '256 are not light detectors, but instead are thermal detectors. As far as Applicant can determine, Watton '256 does not teach the first and second regions recited in claim 1, so that there can be a first bump interconnect and second bump interconnect as recited in claim 1. Thus, neither Ozaki nor Watton '256 teach this fundamental limitation of the structure of claim 4.

Claim 8 recites in part:

> "a first bump interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and

"a second bump interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element."

Referring to the sentence bridging pages 4-5 of the final Office Action, the portion of Ozaki that is read upon the claimed "first semiconductor region" is the n-type layer 3, and the portion of Ozaki that is read upon the claimed "second semiconductor region is the p-type layer 2. Applicant certainly agrees that there is a "second bump" 8 interconnect extending to the p-type layer 2, as shown in Figure 2(c) of Ozaki.

But there is no "...first bump interconnect extending...to the first region..." as recited in claim 1. The n-type layer 3 is not even shown in Figure 2(c) of Ozaki, so none of the bumps 8 or 8A or 8B can extend to the n-type layer 3. The argument presented at page 10, lines 13-18 of the final Office Action is a construct that is unsupported in the facts. There is no disclosure or illustration suggesting that any of the bumps 8, 8A, or 8B extend to, contact, reach or otherwise have any relation to the n-type layer 3. The response asserts that the bump 8 "simply reaches the area of the first region", but a look at Figure 2(c) tells you it doesn't--nothing suggests that any of the bumps 8 reach the n-type layer 3 shown only in Figure 2(b), and in fact all of the bumps 8 terminate at the p-type layer 2.

The explanation of the rejection seeks to focus on Figures 2a-c, and to capitalize on the possible ambiguity permitted by the fact that Figures 2a and 2b show the n-type layer 3, while Figure 2c does not. Of course, because Figure 2c does not show the n-type layer 3, it cannot be presumed to have any particular relation to the bumps 5, and there can be no presumption that any of the bumps 5 connect to the n-type layer 3.

Further light is shed on the question of whether any of the bumps 5 extend to the n-type layer 3 by referring to the embodiment of Figure 4b, which does show both the n-type layer 3 and the p-type layer 2. As may be clearly seen in Figure 4b, the bumps 5 extend only to the p-type layer 2. None of the bumps 5 extend to the n-type layer 3.

"Extend" means "to reach, as to a particular point". The claim language recites the particular points: "a first bump interconnect extending from the first supported-

structure interconnect location...to the first region of its respective supported element". "Reach" means "to succeed in touching", or "to stretch or extend so as to touch or meet" (All definitions set forth herein are evidentiary submissions from Webster's Unabridged Dictionary of the English Language, Portland House, 1989, and the relevant pages were submitted during prosecution). The first bump 8 never touches the n-type layer 3 in Ozaki. It touches the p-type layer 2, but never the n-type layer 3. The bump 8 never extends to the n-type layer 3 under any formal or common-sense definition or concept.

Claim 9 stands or falls with claim 8.

Claim 10 recites in part: "an electrically nonconducting support material lying between the readout integrated circuit array and the detector array". The explanation of the rejection asserts (paragraph bridging pages 4-5 of final Office Action) that element 6 of Ozaki is the circuit array, and that element 1 is the detector. It then goes on to argue that the "electrically nonconducting support material" is element 7 of Ozaki (page 5, lines 13-14 of final Office Action). But it is clear from Figure 2(c) that element 7 of Ozaki is not between elements 6 and 1, as would be required for Ozaki to teach this limitation.

Claim 11 recites in part: "an electrical conductor interconnecting all of the first detector interconnect locations". The final Office Action admits that Ozaki and Watton et al. do not teach any such structure, see the sentence bridging pages 8-9. The rejection is built upon an argument that the recited structure is "well known". Applicant traversed this assertion in a timely manner, but there was no further application of prior art to support the rejection. Battersby '044 is mentioned (final Office Action, page 12, lines 3-12) but not applied in forming the rejection, and therefore cannot be relied upon. Battersby '044 is also a strange reference to attempt to rely upon in relation to what is "well known" about Ozaki's teachings and Watton's teachings. Ozaki teaches a bump interconnect structure in an infrared detector. Watton teaches an interconnect structure in a thermal detector. Like Bryan '547, Battersby '044 has nothing to do with bump interconnect structures, infrared detectors, or thermal detectors, and has no teaching about any of these subjects. Battersby '044 teaches amorphous silicon photodiodes (col. 4, lines 19-21), with no mention of any other type of detector structure. So

Battersby '044 certainly does not support any assertion of what is "well known" in respect to bump interconnect structures in infrared detectors, as taught by Ozaki. There is no objective basis stated for attempting to combine teachings of Battersby '044 with Ozaki and Watton.

Claim 12 recites in part: "the readout integrated circuit array and the detector array are each substantially planar". Ozaki has no such teaching. The recited "hybrid microelectronic array structure" includes the microelectronic integrated circuit array, the supported array, and the bump interconnect structure. Nowhere does Ozaki teach or illustrate that the structure formed of these three elements is planar. In each case taught by Ozaki, the element that corresponds to the supported array has a quasi curvature. The element that corresponds to the supported array is planar. The explanation of the rejection points to Figure 1 of Ozaki, but that structure is clearly not planar, because the supported array is curved.

Claim 13 recites in part: "the readout integrated circuit array and the detector array are each curved". Ozaki has no such teaching. The recited "hybrid microelectronic array structure" includes the microelectronic integrated circuit array, the supported array, and the bump interconnect structure. Nowhere does Ozaki teach or illustrate that the structure formed of these three elements is curved. In each case taught by Ozaki, the element that corresponds to the supported array has a quasi curvature. The element that corresponds to the supported array is planar. The explanation of the rejection points to Figure 1 of Ozaki, but that structure is clearly not curved, because the microelectronic integrated circuit array is planar.

Claim 14 recites in part: "the first bump interconnect and the second bump interconnect each comprise the element indium". As discussed earlier in the discussion of the rejection of claim 8, there is no "first bump interconnect" taught by Ozaki that meets the limitations of claim 8, and therefore there can be no teaching that the first bump interconnect of claim 14 comprises indium.

Claim 15 stands or falls with claim 8.

Claim 16 recites in part: "each of the detector islands is electrically isolated from each of the other detector islands except through the readout integrated circuit

array". The elements 1 are asserted by the explanation of the rejection to be the detector islands. Ozaki teaches directly to the contrary, stating in the Abstract under Constitution, "The pieces of the divided substrate 1 are joined together making cut surfaces butt against each other..." [emphasis added]. That is, after the substrate 1 is cut, the cut pieces are joined together by making the cut surfaces butt against each other. The detector islands therefore are not electrically isolated from each other, because they are joined together in this manner.

Claim 16 further recites in part:

> "a first interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and
>
> "a second interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element."

Referring to the paragraph bridging pages 6-7 of the final Office Action, the portion of Ozaki that is read upon the claimed "first semiconductor region" is the n-type layer 3, and the portion of Ozaki that is read upon the claimed "second semiconductor region is the p-type layer 2. Applicant agrees that there is a "second bump" 8 interconnect extending to the p-type layer 2, as shown in Figure 2(c) of Ozaki.

But there is no "...first bump interconnect extending...to the first region..." as recited in claim 1. The n-type layer 3 is not even shown in Figure 2(c) of Ozaki, so none of the bumps 8 or 8A or 8B can extend to the n-type layer 3. The argument presented at page 10, lines 13-18 of the final Office Action is a construct that is unsupported in the facts. There is no disclosure or illustration suggesting that any of the bumps 8, 8A, or 8B extend to, contact, reach or otherwise have any relation to the n-type layer 3. The response asserts that the bump 8 "simply reaches the area of the first region", but a look at Figure 2(c) tells you it doesn't--nothing suggests that any of the bumps 8 reach the n-type layer 3 shown only in Figure 2(b), and in fact all of the

bumps 8 terminate at the p-type layer 2.

The explanation of the rejection seeks to focus on Figures 2a-c, and to capitalize on the possible ambiguity permitted by the fact that Figures 2a and 2b show the n-type layer 3, while Figure 2c does not. Of course, because Figure 2c does not show the n-type layer 3, it cannot be presumed to have any particular relation to the bumps 5, and there can be no presumption that any of the bumps 5 connect to the n-type layer 3.

Further light may be shed on the question of whether any of the bumps 5 extend to the n-type layer 3 by referring to the embodiment of Figure 4b, which does show both the n-type layer 3 and the p-type layer 2. As may be clearly seen in Figure 4b, the bumps 5 extend only to the p-type layer 2. None of the bumps 5 extend to the n-type layer 3.

"Extend" means "to reach, as to a particular point". The claim language recites the particular points: "a first bump interconnect extending from the first supported-structure interconnect location...to the first region of its respective supported element". "Reach" means "to succeed in touching", or "to stretch or extend so as to touch or meet" (All definitions set forth herein are evidentiary submissions from Webster's Unabridged Dictionary of the English Language, Portland House, 1989, and the relevant pages were submitted during prosecution). The first bump 8 never touches the n-type layer 3 in Ozaki. It touches the p-type layer 2, but never the n-type layer 3. The bump 8 never extends to the n-type layer 3 under any formal or common-sense definition or concept.

Claim 17 stands or falls with claim 16.

Claim 18 recites in part:

> "forming on each detector element a first interconnect to the first semiconductor region and a second interconnect to the second semiconductor region"

Referring to the paragraph bridging pages 7-8 of the final Office Action, the portion of Ozaki that is read upon the claimed "first semiconductor region" is the n-type layer 3, and the portion of Ozaki that is read upon the claimed "second semiconductor

region" is the p-type layer 2. Applicant certainly agrees that there is a connection to the second semiconductor region extending to the p-type layer 2, as shown in Figure 2(c) of Ozaki.

But there is no step of "forming...a first interconnect to the first semiconductor region..." as recited in claim 18. The n-type layer 3 is not even shown in Figure 2(c) of Ozaki, so none of the bumps 8 or 8A or 8B can extend to the n-type layer 3. The argument presented at page 10, lines 13-18 of the final Office Action is a construct that is unsupported in the facts. There is no disclosure or illustration suggesting that any of the bumps 8, 8A, or 8B extend to, contact, reach or otherwise have any relation to the n-type layer 3. The response asserts that the bump 8 "simply reaches the area of the first region", but a look at Figure 2(c) tells you it doesn't--nothing suggests that any of the bumps 8 reach the n-type layer 3, and in fact all of the bumps 8 terminate at the p-type layer 2. In fact, all that is needed is to count that there are 6 bumps 8 on the bottom in each group of Figure 2(c), and a corresponding 6 bumps 5 on the top in each group. Figure 2(c) clearly indicates that the 6 bumps 5 on the top are in communication with the p-type layer 2, leaving no top bumps for communication with the n-type layer 3.

The explanation of the rejection seeks to focus on Figures 2a-c, and to capitalize on the possible ambiguity permitted by the fact that Figures 2a and 2b show the n-type layer 3, while Figure 2c does not. Of course, because Figure 2c does not show the n-type layer 3, it cannot be presumed to have any particular relation to the bumps 5, and there can be no presumption that any of the bumps 5 connect to the n-type layer 3.

Further light is shed on the question of whether any of the bumps 5 extend to the n-type layer 3 by referring to Figure 4b, which does show both the n-type layer 3 and the p-type layer 2. As may be clearly seen in Figure 4b, the bumps 5 extend only to the p-type layer 2. None of the bumps 5 extend to the n-type layer 3.

"Extend" means "to reach, as to a particular point". The claim language recites the particular points: "a first bump interconnect extending from the first supported-structure interconnect location...to the first region of its respective supported element". "Reach" means "to succeed in touching", or "to stretch or extend so as to touch or meet"

(All definitions set forth herein are evidentiary submissions from Webster's Unabridged Dictionary of the English Language, Portland House, 1989, and the relevant pages were submitted during prosecution). The first bump 8 never touches the n-type layer 3 in Ozaki. It touches the p-type layer 2, but never the n-type layer 3. The bump 8 never extends to the n-type layer 3 under any formal or common-sense definition or concept.

Claim 18 further recites in part: "depositing the first semiconductor region onto a detector substrate". At page 7, line 17, the explanation of the rejection asserts that the element 9 of Ozaki is the "detector substrate". Element 9 of Ozaki is a press fixture that is brought in briefly to assist in the press bonding of the bumps and then pulled back, not a "detector substrate". See para. [0024] of Ozaki.

Claim 19 recites in part: "the first interconnect and the second interconnect of each interconnect structure are each electrically conducting bump interconnects". There is no first interconnect in the approach of Ozaki, and therefore there is no first interconnect that may be an electrically conducting bump.

Claim 20 recites in part: "forming a trench through the first semiconductor region and through the second semiconductor region and into the detector substrate". Ozaki has no such teaching for two reasons. First, the "cut" in Ozaki is not a "trench". The "cut" in Ozaki severs two pieces from one another. The "trench" in the present approach does not sever two pieces from one another, but only goes part way through the detector substrate so that the two pieces are not severed. In the present application, see the trench 52 of Figure 5 and its discussion in para. [0034], and the trench 74 of Figure 10 and its discussion at para. [0041]. Second, there is no teaching in Ozaki that the cut passes through the n-type layer 3, which is analogized in the explanation of the rejection to the first semiconductor region of the claims. Thus, Ozaki does not teach "forming a trench through the first semiconductor region..."

Claim 21 recites in part: "an additional step, after the step of preparing and before the step of joining the detector array, of removing the detector substrate.". The explanation of the rejection suggests that this step is illustrated in the change from Figure 3a to Figure 3b in Ozaki. The change between these two figures is that elements 9 and 11 are removed. Neither element 9 nor element 11 is a "detector substrate".

Element 9 is a "press fixture", see para. [0024] of Ozaki, and element 11 is also a "press fixture", see para. [0025] of Ozaki. The function of the press fixtures 9 and 11 in Ozaki is to perform the bonding of the bumps 5 and 8, and therefore the fixtures 9 and 11 cannot be removed "before the step of joining the detector array", as recited in claim 21.

Claim 22 recites in part: "an additional step, after the step of joining, of deforming the hybrid microelectronic array structure into a curved geometry". .The "step of joining" refers back to claim 18, where the step of joining of the interconnects, which are preferably the bump contacts. The explanation of the rejection (final Office Action, page 8, lines 12-13) refers to Figures 3a and 3b to support the rejection. Figures 3a and 3b clearly show that the deforming operation of the detector elements 1 and 2 of Ozaki occurs before, not after, the joining. In Figure 3a, the deforming of a part of the structure into a curved shape is complete, but the bumps 5 and 8 are still not joined. The entire structure of Ozaki is never deformed into a curved geometry.

Claim 23 recites in part: "the readout integrated circuit array comprises an electrical conductor interconnecting all of the first detector interconnect locations." The final Office Action admits that Ozaki and Watton et al. do not teach any such structure, see sentence bridging pages 8-9. The rejection is built upon an argument that, despite the fact that the only applied references do not teach the limitation, the recited structure is "well known". Applicant traversed this assertion in a timely manner, but there was no further application of prior art to support the rejection. Battersby '044 is mentioned (final Office Action, page 12, lines 3-12) but not applied in forming the rejection, and therefore cannot be relied upon. As noted earlier, Battersby '044 is a strange reference to attempt to rely upon in relation to what is "well known" about the admitted lack of the required teachings in Ozaki and Watton. Ozaki teaches a bump interconnect structure in an infrared detector. Watton teaches an interconnect structure in a thermal detector. Battersby '044 has nothing to do with bump interconnect structures, infrared detectors, or thermal detectors, and has no teaching about any of these subjects. Battersby '044 teaches amorphous silicon photodiodes (col. 4, lines 19-21), with no mention of any other type of detector structure. So Battersby '044 certainly does not support any assertion of what is "well known" in respect to bump interconnect structures

in infrared detectors, as taught by Ozaki. There is no objective basis stated for attempting to combine teachings of Battersby '044 with Ozaki and Watton.

Applicant incorporates the discussion of the need for an objective basis for combining the teachings of the references into this Issue 2.

Issue 3. Is claim 5 properly rejected under 35 USC 103 over Ozaki in view of Shieh '225?

Claim 5 recites in part: "the electrical interface circuit is a driver integrated circuit, and the input/output element is an emitter".

The stated rejection is a combination of the teachings of Ozaki and Shieh. Ozaki teaches a light detector (see title), and Shieh teaches a light emitter (see title). The explanation of the rejection argues that it would have been obvious to "...utilize emitters and driver integrated circuits as taught by Shieh et al. for the structure of Ozaki et al..." This statement is without a logical basis--the light detector structure of Ozaki does not use an emitter or a driver integrated circuit. If the argument is that it would be obvious to completely change the functionality of Ozaki and render Ozaki inoperable by replacing the detector of Ozaki with the emitter of Shieh, Applicant must strongly disagree. MPEP 2143.01 provides that, in constructing a sec. 103 rejection, the proposed modification cannot render the prior art unsatisfactory for its intended purpose or change the principle of operation of a reference. MPEP 2143.02 requires that, in combining the teachings of two references, there must be a reasonable expectation of success in the combination. Both of these mandates would be violated in the proposed approach of replacing the detector of Ozaki with the emitter electronics of Shieh. The detector approach required and taught by Ozaki would be rendered unsatisfactory for its intended purpose if some elements were removed and replaced by a light emitter. The detector of Ozaki would be rendered inoperable if its electronics were replaced by the emitter and driver integrated circuits of Shieh.

Applicant incorporates the discussion of the need for an objective basis for combining the teachings of the references into this Issue 3.

Summary and Conclusion

The rejections are based on adding teachings and structure into Ozaki that simply are not there in the printed reference. The stated rejections therefore do not meet the fundamental requirement for a prima facie rejection. Other recited limitations are not taught as well, and the legal requirements for the rejections are not met.

Applicant asks the Board to reverse the rejections.

Respectfully submitted,
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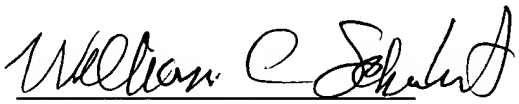

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APPENDIX

Clean Copy of Appealed Claims

1. A hybrid microelectronic array structure comprising:

a microelectronic integrated circuit array comprising an array of microelectronic integrated circuits, each of the microelectronic integrated circuits comprising a first supported-structure interconnect location and a second supported-structure interconnect location;

a supported array comprising an array of supported islands with each supported island having at least one supported element therein, there being at least one supported element for each of the microelectronic integrated circuits, each of the supported elements comprising a first region and a second region, wherein

the first region of each of the supported islands is physically discontinuous from the first region of each of the other supported islands, and

the second region of each of the supported islands is physically discontinuous from the second region of each of the other supported islands; and

a bump interconnect structure extending between each of the microelectronic integrated circuits and its respective supported element, each bump interconnect structure comprising

a first bump interconnect extending from the first supported-structure interconnect location of each of the microelectronic integrated circuits to the first region of its respective supported element, and

a second bump interconnect extending from the second supported-structure interconnect location of each of the microelectronic integrated circuits to the second region of its respective supported element.

2. The hybrid microelectronic array structure of claim 1, wherein the first region comprises a first semiconductor region and the second region comprises a second semiconductor region.

3. The hybrid microelectronic array structure of claim 1, wherein each microelectronic integrated circuit comprises

an electrical interface circuit, and

wherein each supported element comprises

an input/output element supported on the electrical interface circuit.

4. The hybrid microelectronic array structure of claim 3, wherein

the electrical interface circuit is a readout integrated circuit, and

the input/output element is a detector.

5. The hybrid microelectronic array structure of claim 3, wherein

the electrical interface circuit is a driver integrated circuit, and

the input/output element is an emitter.

6. The hybrid microelectronic array structure of claim 1, wherein the hybrid microelectronic array structure is planar.

7. The hybrid microelectronic array structure of claim 1, wherein the hybrid microelectronic array structure is curved.

8. A hybrid microelectronic array structure comprising:

a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being at least one respective detector element for each of the readout integrated circuits, each of the detector elements comprising a first semiconductor region and a second semiconductor region, wherein

the first semiconductor region of each of the detector islands is physically discontinuous from the first semiconductor region of each of the other detector islands,

and

the second semiconductor region of each of the detector islands is physically discontinuous from the second semiconductor region of each of the other detector islands; and

a bump interconnect structure extending between each of the readout integrated circuits and its respective detector element, each bump interconnect structure comprising

a first bump interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and

a second bump interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element.

9. The hybrid microelectronic array structure of claim 8, wherein

the first semiconductor region of each of the detector islands is an n-doped semiconductor, and

the second semiconductor region of each of the detector islands is a p-doped semiconductor.

10. The hybrid microelectronic array structure of claim 8, wherein the hybrid microelectronic array structure further comprises

an electrically nonconducting support material lying between the readout integrated circuit array and the detector array.

11. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array comprises

an electrical conductor interconnecting all of the first detector interconnect locations.

12. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array and the detector array are each substantially planar.

13. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array and the detector array are each curved.

14. The hybrid microelectronic array structure of claim 8, wherein the first bump interconnect and the second bump interconnect each comprise the element indium.

15. The hybrid microelectronic array structure of claim 8, wherein the detector array type is selected from the group consisting of mercury-cadmium-telluride, indium antimonide, quantum well infrared photodetector, and extrinsic impurity band conductor material.

16. A hybrid microelectronic array structure comprising:

a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being at least one respective detector element for each of the readout integrated circuits, each of the detector elements comprising a first semiconductor region and a second semiconductor region, and wherein each of the detector islands is electrically isolated from each of the other detector islands except through the readout integrated circuit array; and

an interconnect structure extending between each of the readout integrated circuits and its respective detector element, each interconnect structure comprising

a first interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and

a second interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element.

17. The hybrid microelectronic array structure of claim 16, wherein the first interconnect and the second interconnect of each interconnect structure are each electrically conducting bump interconnects.

18. A method of fabricating a hybrid microelectronic array structure, comprising the steps of

providing a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

preparing a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being a respective detector element for each of the readout integrated circuits, each of the detector islands comprising a first semiconductor region and a second semiconductor region, the step of providing a detector array including the steps of

depositing the first semiconductor region onto a detector substrate and depositing the second semiconductor region onto the first semiconductor region,

defining detector islands as electrically isolated segments, each detector island including a segment of the first semiconductor region overlying the detector substrate, and the second semiconductor region overlying the first semiconductor region,

forming on each detector element a first interconnect to the first semiconductor region and a second interconnect to the second semiconductor region; and

joining the detector array to the readout integrated circuit array by an interconnect structure to form the hybrid microelectronic array structure, with each readout integrated electrically interconnected to the respective one of the detector

elements, the step of joining including the steps of

joining each first interconnect to the respective first detector interconnect location, and

joining each second interconnect to the respective second detector interconnect location.

19. The method of claim 18, wherein the first interconnect and the second interconnect of each interconnect structure are each electrically conducting bump interconnects.

20. The method of claim 18, wherein the step of defining detector islands includes the step of

forming a trench through the first semiconductor region and through the second semiconductor region and into the detector substrate.

21. The method of claim 18, including an additional step, after the step of preparing and before the step of joining the detector array, of

removing the detector substrate.

22. The method of claim 18, including an additional step, after the step of joining, of

deforming the hybrid microelectronic array structure into a curved geometry.

23. The method of claim 18, wherein the readout integrated circuit array comprises

an electrical conductor interconnecting all of the first detector interconnect locations.